

**APPLICATION FOR
UNITED STATES PATENT
IN THE NAME OF**

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OF

**HIGH SPEED SOURCE SYNCHRONOUS SIGNALING FOR
INTERFACING VLSI CMOS CIRCUITS TO TRANSMISSION LINES**

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HIGH SPEED SOURCE SYNCHRONOUS SIGNALING FOR INTERFACING VLSI

CMOS CIRCUITS TO TRANSMISSION LINES

PRIORITY REFERENCE TO PROVISIONAL APPLICATION

- 5 This application is a continuation of US patent application serial number 09/475,087, which is a divisional of US patent 6,160,423, issued on December 12, 2000, which claims priority to provisional application serial number 60/078,213, each of which is hereby incorporated by reference.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to computer signal communication, and more particularly to an integrated circuit interface and method for high speed block transfer signaling of data, control and address signals between multiple integrated circuits on a bus or point-to-point with reduced power consumption.

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2. Description of the Background Art

Semiconductor integrated circuits used in digital computing and other digital applications often use a plurality of Very Large Scale Integration (VLSI) interconnected circuits for implementing binary communication across single or multi-segmented transmission lines. Conventional transmission lines include traces, which are formed on a suitable substrate, such as a printed circuit board. Each transmission line may be designed, for example, using so-called micro-strip traces and strip line traces to form a

transmission line having a characteristic impedance on the order of about 50-70 ohms.

Alternatively, each transmission line may have its opposite ends terminated in their characteristic impedance. The output load on a driver for such a transmission line may be as low as 25-35 ohms.

- 5 To consume reasonable power, high frequency signaling requires small amplitude signals. For a receiver to detect voltage swings (e.g., 0.8v to 1.2v) easily in a noisy environment like GTL, HSTL, SSTL or RAMBUS, the current must also be very large (e.g., on the order of 50 to 60 millamps per driver). A typical receiver uses a comparator with a voltage reference (VREF) signal configured midway between input high voltage
- 10 (VIH) and input low voltage (VIL). The VREF signal is a high impedance DC voltage reference which tracks loosely with power supplies over time, but cannot respond to instantaneous noise. Conventionally, High Output Voltage (VOH) and Low Output Voltage (VOL) denote signals emerging from the transmitting source, and VIL and VIH denote signals arriving at the input of the receiving device, although they can be
- 15 considered the same signal.

FIG. 1A is a block diagram illustrating a prior art receiver 10 using RAMBUS technology. The system 10 includes a pad 100 coupled via signal lines 103 to internal input receivers 110. A VREF signal 105 is coupled to each internal receiver 110. VREF is generated from the power supply. Usually, the DC value of the power supply varies by

20 five percent (5%). FIG. 1B is a timing diagram 125 illustrating an example signal relative to a high reference voltage (VREFh) and a low reference voltage (VREFl). The VREFh and VREFl values typically depend on power supply variation used to generate the VREF signal. The large voltage swing, i.e., the difference between a high voltage signal (VIH)

and a low voltage signal (VIL), and stable signal levels above and below the VREF signal are required for reliable detection of signal polarity. The voltage swing of current single-ended signaling technologies is conventionally around 0.8v.

FIG. 1C is a block diagram illustrating schematics of a prior art receiver 150 using
5 RAMBUS technology. The receiver 150 samples the level of input signal 167 and of the
VREF signal 154 until the signal reaches a stable level, at which time the pass gates 160
and 165 turn off. Once the pass gates 160 and 165 turn off, the sense gate 172 is enabled
to eliminate current injection. FIG. 1D is a timing diagram 175 illustrating operation of
the receiver 150 for an example signal. The receiver 150 samples the input reference and
10 input signal until the signal reaches a stable level, e.g., a low logic level (VIL), and, while
the input signal is stable, the receiver 150 senses the value of the input signal. As stated
above, for reliable signal detection, the signal voltage swing must be fast to allow all the
receivers 150 to sample a stable signal with an adequate margin for set-up and hold time.
This voltage swing should occur in less than 30% of the minimum cycle time to allow
15 margin for signal skew, set-up and hold-times. As the minimum cycle time reduces below
1 nanosecond, the margins reduce for signal skew, set-up time and hold-time, with the
additional burden on the driver current in a high capacitance loading environment
operating at high frequency. Low voltage differential signaling (LVDS) used by IEEE
P1596.3 can overcome these problems by using a 250mv voltage swing at the expense of
20 running complimentary signals. Running complementary signals inevitably increases the
pin count and package size.

Accordingly, there is a need for low power drivers and reliable receivers for high frequency operation of a large number of single-ended signals in existing technology for low cost VLSI digital systems.

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SUMMARY AND OBJECTS OF THE INVENTION

A system of the present invention uses small swing differential source synchronous voltage and timing reference signals (SSVTR and /SSVTR) to compare single-ended signals of the same swing generated from the same integrated circuit for high frequency signaling. It will be appreciated that “/” is being used to indicate a logical

10 NOT. All signals are terminated with their characteristic impedance on both ends of the transmission lines. SSVTR and /SSVTR toggle every time the valid signals are driven by the transmitting integrated circuit. Each signal receiver includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR. A present signal binary value determines which comparator is coupled, 15 optionally by using exclusive-OR logic with SSVTR and /SSVTR. Until SSVTR and /SSVTR have changed their binary value, the coupled comparator in the receiver detects whether a change in signal binary value occurred. Again, it will be appreciated that SSVTR and /SSVTR change their binary value every time the signal can change its binary value. SSVTR and /SSVTR are preferably synchronized with the signal.

20 The method of the present invention includes the steps of obtaining an oscillating source synchronous voltage and timing reference and its complement (SSVTR and /SSVTR), and receiving an incoming single-ended signal. The method compares the oscillating reference against the incoming signal by a first comparator to generate a first

result, and compares the complement against the incoming signal by a second comparator to generate a second result. The method then selects one of the first result or the second result as an output signal based on the previous signal. The step of selecting one of the results includes comparing the output signal to the reference (SSVTR) and to the 5 complement (/SSVTR). The step of selecting further includes manipulating the output signal from the previous signal towards the first result or second result, based on the comparator which is currently coupled. If the incoming signal changes, the step of selecting includes maintaining the same comparator coupled. If the incoming signal stays the same, the step of selecting includes de-coupling the currently coupled comparator and 10 coupling the other comparator. The method then allows the circuit to stabilize.

The system and method advantageously eliminate the need for a high impedance VREF signal for comparison of small swing single-ended signals. This reduces the need for three distinct voltage levels (the output high level, output low level and the VREF level) to two distinct voltage levels (the output high level and the output low level). 15 Eliminating VREF reduces necessary voltage swing and accordingly reduces power consumption. Using a receiver with dual comparators allows coupling of the receiver to the same comparator when the signal changes every cycle. Only one comparator is coupled based on the current binary value of the signal and SSVTR. The system has an individually adjustable delay for each receiver to couple or de- couple the comparator, 20 thereby reducing the effect of skew during transmission of source synchronous signals.

The system may have multiple differential source synchronous voltage and timing reference signals to compare multiple single-ended signals in the same integrated circuit

such as a microprocessor or system controller that has many signals. The system and method provide differential signaling benefits in a single-ended signaling system.

Using the same concept, the system may have bi-directional complementary source synchronous voltage and timing reference signals to compare bi-directional single-ended signals. The system may have a driver or transmitter for controlling the signal slew rate to be a substantial portion the total signal period, thereby reducing output current. The system may have internal impedance matching circuitry such as pull-up resistors or grounded gate p-channel for matching the characteristic impedance of the transmission line on both ends of a point-to-point connection between CPU and cache or CPU and system controller. The system has a dual comparator circuit to convert a single-ended bus with two complimentary signals to be transmitted and received with comparable noise immunity of differential bus for internal data bus of memory, processor or other wide data bus type integrated circuits. The system preferably has variable device size of the transmitter with slow turning-on and slow turning-off to have similar slew rates for all signals in each group of SSVTR and /SSVTR and plurality of signals which are transmitted together.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a block diagram illustrating a prior art RAMBUS-based receiver.

20 FIG. 1B is a timing diagram illustrating signal levels of the FIG. 1A prior art receiver.

FIG. 1C is a schematic diagram illustrating another prior art RAMBUS-based receiver.

FIG. 1D is a timing diagram illustrating operation of the FIG. 1C prior art receiver.

FIG. 2A is a perspective view block diagram illustrating a system with a master and slave devices in accordance with the present invention.

5 FIG. 2B is a block diagram illustrating the FIG. 2A system having transmission lines with impedance matching resistors at the ends.

FIG. 3A is a timing diagram illustrating the differential reference signals SSVTR and /SSVTR relative to signal sense times.

10 FIG. 3B is a timing diagram illustrating SSVTR and /SSVTR relative to a single-ended signal.

FIG. 4 is a high level schematic illustrating single-ended signal receivers.

FIG. 5 is a flowchart illustrating a method of communicating signals from a transmitter across a transmission line to a receiver.

15 FIG. 6A is a schematic diagram illustrating a slow turning-on and slow turning-off driver for all signals.

FIG. 6B is a schematic diagram illustrating drivers having adjustable signal slew rates and skew between signals.

FIG. 7A is a schematic diagram illustrating a FIG. 4 single-ended signal receiver in a first embodiment.

20 FIG. 7B is a schematic diagram illustrating a FIG. 4 single-ended signal receiver in a second embodiment.

FIG. 7C is a schematic diagram illustrating a FIG. 4 single-ended signal receiver in a third embodiment.

FIG. 7D is a schematic diagram illustrating a FIG. 4 single-ended signal receiver in a fourth embodiment.

FIG. 8A is a schematic diagram illustrating circuit details of the SSVTR to /SSVTR comparator of FIG. 4.

5 FIG. 8B is a schematic diagram illustrating circuit details of the /SSVTR to SSVTR comparator of FIG. 4.

FIG. 9 is a schematic diagram illustrating receivers with individually adjustable delays to eliminate skew during transmission.

10 FIG. 10 illustrates signal waveforms and skew between them.

FIG. 11 is a perspective view of a hard-wire layout of the FIG. 2 system.

FIG. 12A is a block diagram illustrating a point-to-point system in accordance with this invention.

15 FIG. 12B is a block diagram illustrating the FIG. 12A point-to-point connection having impedance-matching grounded gate p-channel devices inside the integrated circuit.

FIG. 13A is a perspective view block diagram illustrating a unidirectional signaling system and a bi-directional signaling system on a single integrated circuit.

FIG. 13B is a perspective view block diagram illustrating four signaling systems on a single integrated circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a signaling system and method for high-speed communication on multiplexed bus or point-to-point connections between multiple VLSI devices with lower power consumption relative to current methodology of interfacing 5 single-ended signals. The signaling system can be used to connect multiple memory devices with a multiplexed bus to a memory controller for block transfer of data, addresses and control information. By using multiple buses, devices such as DRAMs, cross-point switches, processors, wide SRAMs and System controllers can be put together to achieve bandwidths above four gigabytes/sec. Virtually all of the signals needed for 10 computer or other digital systems can be sent over this bus. Persons skilled in the art will recognize that all devices like CPUs in the computer system need include the methodologies and bus structures of this system.

FIG. 2A is a perspective view block diagram illustrating a system 200 with a master device (transmitters) 205 coupled via a bus architecture (transmission lines) 215 to 15 multiple slave devices (receivers) 210 in accordance with the present invention. An example of a master device 205 and slave device 210 pair includes a microprocessor and system controller, or a memory controller and memory device (e.g., DRAM). As illustrated, the master 205 is configured to communicate, for example, twenty (20) signals including single-ended signals S0 to S17, small swing complementary source 20 synchronous voltage and timing references SSVTR and /SSVTR, power lines (not shown) and ground lines (not shown) in parallel via transmission lines 215 to each slave 210. It will be appreciated that “/” is being used to indicate a logical NOT. The signals S0- S17 can be data, control or addresses either multiplexed or non-multiplexed as defined by the

protocol. There may be additional signals like clock or initialization for other purposes required by the protocol or synchronization of system.

As shown in FIG. 3A, the SSVTR and /SSVTR signals toggle every time the valid signals are driven by the master 205. It will be appreciated that slave 210 may include 5 multiple receivers (405, FIG. 4), wherein each receiver 405 includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR. A present signal binary value determines which comparator is coupled to the output terminal 420, optionally by using exclusive-OR logic with SSVTR and /SSVTR. Until SSVTR and /SSVTR have changed their binary value, the enabled 10 comparator in the receiver 405 detects whether change in signal binary value occurred.

For chip-to-chip communication on a bus or point to point, all signals are transmitted preferably at substantially the same time from the same chip to another chip or plurality of chips connected on the bus and preferably have substantially the same loading, swing and slew rate (when the signals are transitioning). Also, for intra-chip 15 communication, the signals are driven preferably at substantially the same time from the same area or block to other areas or other blocks in the same chip and preferably have substantially the same loading, swing and slew rate (when the signals are transitioning)

To facilitate extremely high data transmission rates over this external bus, the bus cycles are initiated when SSVTR is low (i.e., /SSVTR is high). All block transfer begins 20 during the cycle when SSVTR is low and ends with SSVTR going low to ease presetting the receiver 405 for the last binary value of the signal. This allows burst transfers of even number of bits. When the signals need to change direction (due to the multiplex nature of

signals), one or more dead cycles may be required for settling down the bus due to propagation delays or settling of SSVTR and /SSVTR, when they are bi-directional.

FIG. 2B is a block diagram illustrating the system 200 (FIG. 2A) having transmission lines 215 with external impedance matching resistors 220 having 5 termination resistance equal to their characteristic impedance, which is preferably between 50-70 ohms, at the ends. The termination voltage is labeled VTT, which is preferably around 1.8v for a 2.5v operating voltage (for VCC of 2.5V and VSS of 0V). The nominal voltage swing is preferably set less than one volt, preferably less than 40% of the supply voltage, and most preferably set at 500mv. Therefore, as shown in FIG. 3A, 10 the output high voltage (VOH) is 1.8v and output low voltage (VOL) is 1.3v.

FIG. 3A is a timing diagram illustrating the complementary reference signals SSVTR and /SSVTR relative to signal sense times. SSVTR initiates at VOL and /SSVTR initiates at VOH. In the first cycle, the master 205 drives all the low going signals including /SSVTR to VOL at the same time and the termination resistances 220 15 pull up SSVTR to VOH. The single-ended signals that are high are held at VOH by the terminating resistances. Proper sense time, i.e., time to sense the logic level of an input signal, is after the transition junction of SSVTR and /SSVTR and before the stable time, i.e., when the SSVTR or /SSVTR reaches steady state at VIH or at VIL. The SSVTR and /SSVTR preferably have equal rise and fall times, wherein each rise and fall time is 20 approximately half of a cycle time of either reference.

FIG. 3B is a timing diagram illustrating SSVTR and /SSVTR relative to a single-ended signal. The single-ended signal begins equal to /SSVTR at a high voltage, and then transitions with /SSVTR to a low voltage. The single-ended signal then remains at a low

voltage, thereby becoming equal to SSVTR, and then transitions with SSVTR to a high voltage. The single-ended signal then remains at a high voltage, thereby becoming equal to /SSVTR.

Sub by 5

FIG. 4 is a high level schematic illustrating a single-ended signal slave 210, having a receiver 405 for each signal line 215. Each signal receiver 405 has two comparators 410, one comparator 410a for comparing an incoming single-ended signal "SNx" to SSVTR and the other comparator 410b for comparing SNx to /SSVTR. Both of the comparators 410 have output terminals selectively coupled via switches 415 to an output terminal 420. It will be appreciated that the output signal (SN) to the output terminal 420 is preferably a full rail signal (0V to 2.5V).

As stated above, SSVTR is initially set to VOL and /SSVTR and SNx are initially set to VOH. SN is initially set to a full rail high output voltage. Accordingly, the comparator 410a amplifies high voltage SNx minus low voltage SSVTR, thereby providing a high output signal. The comparator 410b amplifies high voltage SNx minus high voltage /SSVTR, providing a noise-amplified unknown output signal. Switch 415 selection is controlled by exclusive-OR (XOR) logic gates 425. More particularly, XOR gate 425a compares a full rail SSVTR amplified signal (VT) against output signal SN, and generates a control signal for controlling switch 415a. XOR gate 425b compares full rail /SSVTR (/VT) against output signal SN, and generates a control signal for controlling switch 415b. In this initial state, only SSVTR and accordingly VT are low, thereby causing XOR 425a to drive switch 415a closed. Accordingly, the comparator 410a output (high) reaches output terminal 420. XOR 425 drives switch 415b open, thereby

preventing the entry of the unwanted output signal from comparator 410b. Receiver 405 is stable.

Following the example illustrated in FIG. 3B, the single-ended signal SNx transitions to a low voltage. As always, SSVTR and /SSVTR transition opposite to one another. Accordingly, as soon as SSVTR and /SSVTR achieve a predetermined difference (preferably 250mV) therebetween, VT and /VT transition. Similarly, as soon as SSVTR and SNx transition to a predetermined difference (preferably 250mV) therebetween, the output of comparator 410a also transitions (to a low output voltage). It will be appreciated that the path from external signal SNx to the generation of output signal SN and the path for full rail signal VT and /VT generation path each include one comparator 410 or 435 and two inverters 430 or 440. Thus, each XOR 425 will receive new input signals based on the speed of the comparison by the comparators 410 and 435. In this example, as evident by the example timing diagram of FIG. 3B, SSVTR and /SSVTR will achieve a predetermined difference at the same time that SSVTR and SNx achieve the same predetermined difference. Accordingly, the XOR 425a will continue to receive differential inputs, thereby maintaining the same switch 415a closed and enabling the low output voltage of comparator 410a to pass to output terminal 420. Receiver 405 is still stable.

Still following the example of FIG. 3B, the single-ended signal SNx does not transition. As always, SSVTR and /SSVTR transition relative to one another. Accordingly, currently enabled comparator 410a continues to drive a low output voltage. When SSVTR and /SSVTR achieve a predetermined difference relative to one another, but before SSVTR reaches the same voltage as SNx (thereby avoiding the possibility of

an undetermined state of the output signal), the XOR 425a switches off and the XOR 425b switches on. It will be appreciated that, from the time /SSVTR began to rise, comparator 410b could drive a low output voltage. Receiver 405 is still stable.

Each receiver 405 can easily detect and amplify very small signals on the order of 5 100-250mV. If the transition has occurred in the single-ended signal SNx, the output signal SN has the new level opposite to its previous signal level. Since both SSVTR (or /SSVTR) and single-ended signals have transitioned, the same comparator 410 is still coupled to the signal output terminal. If the single-ended signals SNx have not transitioned, then the signal output SN does not change, the comparator 410 coupled at 10 the start of the transition is de-coupled from the output after the SSVTR and /SSVTR receiver has amplified their new binary state (VT & /VT), and the other comparator 410 which has opposite /SSVTR (or SSVTR) is coupled to provide the signal output. The old output level is thereby restored.

It will be appreciated that a receiver 405 may be implemented without using 15 XORs. This may be implemented by using the known polarity of SSVTR and /SSVTR in the initial cycle and all single-ended signals starting high. The SSVTR and /SSVTR transition in every cycle. Thus, their polarity in every cycle may be determined by examining the system clock in a synchronous system and defining cycle start in even clock cycles (i.e., SSVTR is low in the even clock cycle and /SSVTR is high). Then, only 20 the output signal "SN" is monitored to couple and de-couple the comparators 410 based upon whether output signal SN changes state every cycle or not. If output signal SN changes state, the coupled comparator is left alone. If the output signal SN does not

change, the coupled comparator is de-coupled and the other comparator is coupled and so on.

It will be further appreciated that a system embodying the invention enables all signals to be connected to low impedance sources, enables all signals to present voltage and noise conditions virtually similar to differential signaling in noise immunity, and

5 enables reduction of voltage swing compared to other single-ended signaling technologies like RAMBUS, HSTL or GTL. The small swing of 0.5v implemented in this exemplary embodiment allows for very high signal rates with much lower power consumption as compared to other existing single-ended signaling technologies. Further, it will be

10 appreciated that each receiver 405 amplifies the single-ended signals SN_x during the transition of the signals without the need of a conventional clock or other timing signal except SSVTR, /SSVTR and their amplified versions VT and /VT.

FIG. 5 is a flowchart a method 500 of communicating signals from a master 205 across a transmission line 215 to a receiver 405. Method 500 begins with the master 205 in step 505 setting SSVTR to VOL and all single-ended signals (/SSVTR and SN_x) to VOH, and in step 510 setting all single-ended receiver outputs (SN) to a full rail high. The receiver 405 in step 515 couples the comparator 410a, which compares SSVTR against each single-ended signal SN_x, to the output terminal 420 of the receiver 405. The receiver 405 in step 517 lets all signals on the transmission lines settle down. Steps 505-

15 20 517 are referred to as system initialization.

The master 205 in step 520 simultaneously drives SSVTR and /SSVTR to their opposite states and all single-ended signals SN_x to their desired levels. The receiver 405 in step 530 compares the single-ended signal SN_x against SSVTR and /SSVTR in

respective comparators 410. The receiver 405 in step 540 determines whether the single-ended signal transitioned. If so, then the receiver 405 in step 545 passes the result to the output terminal 420, and keeps the same comparator 410 coupled to the terminal 420. If not, then the receiver 405 in step 550 decouples the previous comparator 410, couples the other comparator 410 to the output terminal 420, and keeps the same output signal (SN).
5 The transmitter 405 in step 555 determines whether the signal burst continues. If so, then method 500 returns to step 520. Otherwise, method 500 ends.

FIG. 6A is a schematic diagram illustrating a slow turning-on and slow turning-off master 205 for a single-ended signal in a first embodiment referred to as transmitter 600.

10 The transmitter 600 includes an NMOS pull down device 605 coupled to a transmission line 610 for accurately tailoring the output swing to 500mv below VTT. The NMOS pull down device 605 includes a pull down NMOS transistor T1 having its source coupled to the transmission line 610, its drain coupled to ground, and its gate coupled to skew control circuitry 620. The skew control circuitry 620 includes a CMOS inverter, comprising two transistors T2 and T3, coupled between two resistors, R1 and R2. The input to the CMOS inverter is coupled to a signal control device 625. For example, to generate SSVTR or /SSVTR, the signal control device 625 may be an oscillator. It will be appreciated that the amount of pull down can be adjusted using a register (not shown) and a serial pin (not shown) during initialization to set the correct voltage swing for any
15 process or device variations. Other methods like using feedback techniques to control is shown in Hans Schumacher, et al., "CMOS Subnanosecond True-ECL output buffer," J.Solid State Circuits, Vol. 25 (1), pp.150-154 (Feb. 1990) may also be used.
20 Maintaining the current at 20ma and having parallel terminations of 50 ohms on both

ends of the transmission line 610 (as controlled by R1 and R2) generates a 500mv swing under all conditions. To have slow rise and fall times on the output and to minimize reflections, signal coupling and termination network switching noises, the skew control circuitry 665 controls the pull down transistor T1 to turn on and turn off slowly. The 5 preferred slew rate is 1.6ns/volt with transition times of 0.8ns for 500mv.

For a uniformly transitioning ramp-like signal, the preferred slew rate of signals is four times the sum of two inverter delays and an exclusive-OR delay in a given technology. In 0.25μ CMOS technology with an operating voltage of 2.5V, the inverter delay is 50 picoseconds and the exclusive-OR delay is approximately 120 picoseconds.

10 Thus, the preferred slew rate is approximately 880 picoseconds. For signals transmitted above the rate of 600MHz, the signal slew rate is preferably less than 110% of the signal rate. The preferred slew rate for exponential signals is slightly faster if the signal reaches 75% of its final value earlier than $\frac{3}{4}$ of the transition time. The differential signals 15 preferably cross half way through the voltage transition. At around $\frac{3}{4}$ of the way through the voltage transition, the signals have a difference of about 250mv which can be converted quickly to a large swing signal. To avoid noise amplification and to prevent signal coupling to the receiver output upon receipt non-transitioning single-ended signals, the transition time between 75% and the final signal value is preferably higher than the 20 sum of two inverter delays and the exclusive-OR delay. It will be appreciated that the slew rate can go as fast as it takes amplified noise to reach the output of the comparator 410 whose output is coupled to the output terminal 420. That is, upon receiving a non-transitioning signal, the switches 415 switch state before the comparator output changes state based on noise amplification. The output of the currently coupled comparator 410

approaches an undetermined (noise amplified) state. The switches 415 must switch states before the undetermined output becomes available. It will be further appreciated that device mismatches, manufacturing tolerances and signal reflection will effect the speed at which the output of the comparator 410 reaches the undetermined state. As the 5 technology improves, gate delays, faster slew rates and faster signal rates will be achievable.

FIG. 6B is a schematic diagram illustrating master 205 having adjustable signal slew rates and skew between signals, in another exemplary embodiment referred to as transmitter 650. Transmitter 650 includes an NMOS pull down device 655 coupled to the 10 transmission line 610 for accurately tailoring the output swing to 500mv below VTT. The NMOS pull down device 655 includes a pull down NMOS transistors 660 connected in parallel, each having its source coupled to the transmission line 610, its drain coupled to ground, and its gate coupled to skew control circuitry 665. The skew control circuitry 665 includes a CMOS inverter, comprising two transistors T2 and T3, coupled between 15 two sets 670 and 675 of parallel-connected resistors. The input to the CMOS inverter is coupled to the signal control device 625. The resistor sets 670 and 675 tune the rise and fall times. It will be appreciated that the rise and fall times are preferably as symmetric as possible to have midpoint crossover of all signals and sensing of all signals by the differential receivers to occur simultaneously. Achieving symmetry and setting the slew 20 rate and output swing can be achieved during the testing phase by blowing fuses (not shown) or during initialization on board by setting a register (not shown).

It will be appreciated that the signal transition times may be slightly higher than the signal rate. In some heavily loaded buses, the swing can be increased to take care of

transmission losses, still presenting 500mv for the receiver 210 to sense easily. It will be further appreciated that various slew rates, exponential transition times and voltage swings are possible based on technology, loading, and receiver acquisition and resolution delays. Even transition times slightly higher than signal rate are possible with

- 5 transitioning signals reaching 90 to 95% percent of their final value, while bursting. Also during testing the skew between single-ended signals and SSVTR and /SSVTR is adjusted using NMOS pull down size and resistors in the gate prior to it, using well known techniques like laser fuse blowing or setting the register code to achieve the signal waveform shape as shown in FIG. 10. As shown in FIG. 10, all single-ended signals SNx
10 should be coincident or less than 50psec ahead of the SSVTR and /SSVTR transition. This skew may be adjusted after testing to be in this range.

FIGs. 7A-7D illustrate alternative embodiments of each signal receiver 405 of FIG. 4. It will be appreciated that the comparators 410 of receiver 405 need to operate during every cycle, requiring small acquisition and resolution delays, taking no input current and injecting no current back into signal lines. The common differential amplifier satisfies all these requirements. Referring to FIG. 7A, the receiver 210 uses dual differential amplifiers 702, one differential amplifier 702a for comparing the signal SNx to SSVTR and the other differential amplifier 702b for comparing the signal SNx to /SSVTR. For completeness, a brief review of differential amplifiers 702 is provided.

- 15 The differential amplifier 702 is always enabled. Based on channel sizes, when the SSVTR voltage is higher than the SNx voltage, more current is driven across the PMOS transistor T10, thereby pulling the output voltage at node 707 high (close to VCC or 2.5V). When the SSVTR voltage is less than the SNx voltage, more current is drawn

across the NMOS transistor T11, thereby pulling the output voltage at node 707 low (close to VSS or 0V). The differential amplifier converts 0.5V (small swing) input to a large swing (0V to 2.5V) output.

The outputs of the differential amplifiers are amplified and inverted by an inverter 5 704, pass through CMOS transmission gates 706 and are tied together at node 708. The transmission gates 706 are selectively operated depending on the amplified state of previous signal (SN) exclusively-ORed with an amplified state of SSVTR or /SSVTR, i.e. VT or /VT respectively. The exclusive-OR is designed to be stable without glitches for small timing variations between SN, VT and /VT reaching their respective logic levels.

10 Various embodiments are shown. FIG. 7A illustrates an always enabled differential amplifiers with only the transmission gates being selectively enabled for small device count and higher speed as alternative embodiment 700. FIG. 7B illustrates a differential amplifier and the transmission gates being enabled or disabled simultaneously as alternative embodiment 720. FIG. 7C illustrates a differential amplifiers being enabled 15 by the same exclusive-OR for lower power, fast disabling of transmission gates during transition of exclusive-OR output and slow enabling of the transmission gates after the exclusive-OR is settled as alternative embodiment 740. FIG. 7D illustrates a P-channel differential amplifiers with 1.2V termination voltage for lower power applications as alternative embodiment 760. All differential amplifier gates can be disabled for power 20 reduction when the receiver or when the device is not selected or the device is in deep power-down mode. The differential amplifier can be disabled by turning transistor T11 off.

By using a 1.2v termination and receiver 405 as shown in FIG. 7D, the power consumption can be further reduced by another 33%. That is, the voltage swing will be from 1.2V to 0.7V, allowing decent margins from ground bounce and lower power consumption for portable systems. The operating frequency can be comparable with less 5 number of devices on the buses, which is common with portable devices for smaller form factor. The transmitter 205 can still be an NMOS pull down T1 or parallel connection of NMOS pull downs 660. Receiver operation is similar except the differential amplifier 702 becomes a mirror image, thereby increasing the gate capacitance on signals going into the P-channel gate for comparable performance by approximately two times due to 10 the increased device size of the P-channel. Other configurations of differential amplifiers, which convert small swing differential signals to large swing differential signals quickly, may alternatively be used instead of the differential amplifiers shown. One skilled in the art will recognize that another embodiment can use two different VTTs, one for signals equal to 1.8v with 500mv swing and another for oscillating 15 reference signals equal to 1.7V with 300mv swing. All signals transition at the same time and have similar rise and fall times. The same transmitter and receiver pair can manage the multiple VTT system.

It will be appreciated that the DC bias point of each differential amplifier in the receiver 405 is configured so that the receiver 405 output voltage is above half-VCC 20 when both the small swing voltages (single-ended signal SN_x and SSVTR or /SSVTR of the enabled differential amplifier) are close to VIH and below half-VCC when both the small swing voltages are close to VIL. This DC biasing allows for adequate margin and preservation of output signal SN when the single-ended signal SN_x does not change state

and the SSVTR or /SSVTR of the enabled differential amplifier is closing the differential signal before it is de-coupled.

Since the receiver 405 operates during the signal transition for a small swing single-ended signal, the concept of set-up and hold-time from a specified time after the signal level reaches VIH /VIL or VREF in previous signaling techniques no longer applies. Also, there is no VREF (reference voltage) for comparison with the signal voltage. By eliminating the timing necessary for set-up and hold and the timing needed to enable voltage margins for sensing around VREF, the operating frequency is considerably increased with lower power consumption. Further, all receivers 405 are self timed, without the need of a global clock, allowing the receivers 405 to be adjusted individually for elimination of board or package level transmission skew.

FIGs. 8A and 8B are schematic diagrams illustrating circuit details comparators 435 of FIG. 4. Each comparator 435 includes a differential amplifier 802 (FIG. 8A) or 852 (FIG. 8B) similar to the differential amplifier 702 of FIGs. 7A and multiple inverters 804 (FIG. 8A) or 854 (FIG. 8B) in series. The full rail output signals of the comparators 802 and 852 (VT1, VT2, VT3, /VT1, /VT2 & /VT3) are transmitted to all the single-ended receivers' XORs 425 (FIG. 4). Selection of VT1, VT2 or VT3 is determined based on testing for signal speed substantially equal to that of the receiver 405 output signal SN generation path.

FIG. 9 is a schematic diagram illustrating receivers 405 with individually adjustable delays to eliminate skew during transmission and to convert small swing to large swing by comparators 410. To tune the operating frequency or voltage swing for optimum performance, each receiver 405 has a register 905 for storing data to enable

delivery of one of the three VT1 & /VT1, VT2 & /VT2 or VT3 & /VT3 to the XOR 425
(FIG. 4).

FIG. 11 is a perspective view of a hard-wire layout of a combined master 1100 for bi-directional signal communication. The master 1100 includes receivers 405 and return transmitters 1105 coupled together. More particularly, each single-ended signal received such as signal S0 is coupled to a corresponding receiver 405 such as receiver S0 and to a corresponding transmitter 1105 such as transmitter T0. Preferably, all single-ended signals SNx may be grouped together with a single pair of SSVTR and /SSVTR references. However, persons skilled in the art will recognize that, for a given operating frequency, SSVTR and /SSVTR loading and signal imbalance reduce the number of signals SNx that can be grouped together. As shown in FIG. 11, the layout is implemented so that the capacitances, resistances and inductances on SSVTR, /SSVTR and all single-ended signals SNx are balanced. Also, since SSVTR and /SSVTR go to all of the receivers 405, the total loading on SSVTR and /SSVTR needs to be minimized.

15 By using devices with very low power dissipation and close physical packing, the bus can be made as short as possible, which in turn allows for short propagation times and high data rates. As shown in FIG. 2B, the resistor-terminated controlled-impedance transmission lines can operate at signal rates of 1Ghz (1ns cycle). The characteristics of the transmission lines are strongly affected by the loading caused by integrated circuits 20 like DRAMs mounted on the bus. These integrated circuits add lumped capacitance to the lines, which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity of 7.5cm/ns. Care should be taken not to drive the bus

from two devices at the same time. So for buses less than about 12cm, one dead cycle (e.g., 2ns) is needed to settle the bus for switching from one driver to another driver. For longer buses, more than one cycle may be needed for the signals to settle down before a new transmitter can drive the signal. Unlike RAMBUS, the length of the bus does reduce 5 operating frequency in burst mode from the same device.

FIG. 12A is a perspective view block diagram illustrating a point-to-point system 1200, which includes a bi-directional master 1205 coupled via transmission lines 1215 to a bi-directional slave 1210. The transmission lines 1215 includes upper signal SNx lines 1220, lower signal SNx lines 1225 and SSVTR and /SSVTR lines 1230. As illustrated in

10 FIG. 12B is a perspective view block diagram illustrating point-to-point system 1200 incorporating terminating resistances 1235 internally using grounded gate P-channel devices. This eliminates the need for space to connect external resistances and reduces cost. It will be appreciated that the terminating resistances 1235 can be implemented 15 using internal resistors instead of grounded gate P-channel devices. Terminating both ends with the appropriate characteristic impedance is preferable for bi-directional signals on a bus. Since intra-chip blocks are physically proximate, impedance matching resistances are unnecessary. Small pull-up devices are sufficient. Similarly, when interchip connections are physically proximate, impedance matching resistances can be replaced with small pull-up devices to reduce cost and power and to maintain the same 20 slew rate.

It will be appreciated that multiple buses are required for devices like SDRAM, DDR SDRAM or DDR SRAMs, where signals are transmitted and received simultaneously. FIG. 13A is a perspective view block diagram illustrating a combined

- unidirectional and bi-directional system 1300 for SLDRAAM on a single integrated circuit.
- System 1300 includes a master 1305 (e.g., a memory controller) coupled via transmission lines 1315 to slaves 1310 (e.g., SLDRAAMs). The master 1305 transmits address and control signals via address and control lines 1320 and 1325, transmits/receives data
- 5 signals across data lines 1330 and 1335, transmits on SSVTR and /SSVTR lines 1340 a first set of SSVTR and /SSVTR references (i.e., SSVTR0 and /SSVTR0) for examining the address and control signals, and transmits a second set of SSVTR and /SSVTR references (i.e., SSVTR1 and /SSVTR1) to the slaves 1310. The address and control portion of the system 1300 manage unidirectional signals needed only by the slaves 1310.
- 10 The data portion of the system 1300 is bi-directional based on whether the control signal specified a READ or a WRITE operation.
- For an SLDRAAM, the 40-bit command and address is sent in a packet of four 10bit words. SSVTR0 and /SSVTR0, which may be referred to as the system differential clock, operates at 500Mhz. A Phase-Locked Loop (not shown) is used to lock the clock frequency and timing for various internal purposes and driving the data output with 15 SSVTR1 and /SSVTR1 on both edges for a data rate of 1Ghz. All the high frequency signals are terminated on both ends of the bus with their characteristic impedance. The termination on the memory controller end can include external resistances, internal resistances or internal grounded gate P-channel devices, since this memory controller is usually the master and is fixed. Since the number of components (SLDRAAMs) 1310 (which operate like slaves) is variable, components 1310 are preferably terminated by external resistors at the end of the transmission lines. The-18 bit bi-directional data bus 20 1330 and 1335 operates at the same frequency as the system clock for synchronization

and sends data in eight 18-bit words in four clock cycles (8ns) or 2.25 gigabytes/sec from a single SLDARAM. Care is taken to balance the load on SSVTR0 and /SSVTR0 by adding dummy gates and lines to look comparable to SSVTR1 and /SSVTR1. This load balancing makes the slew rate due to loading be similar and allows similar margins for all
5 signals.

When higher bandwidth is required, a system 1350 can use four buses as shown in FIG. 14B. Two separate channels of SLDRAMs 1310 are used with a single memory controller 1305. This configuration allows 4.5 gigabytes/sec peak data bandwidth.

Although the system 1350 does not require synchronous clocks for the transmitter 1305
10 or receiver 1310, the system 1350 can use synchronous clocks to transmit data at a particular time and frequency for ease of testing and usefulness with existing protocols of synchronous DRAMs and SRAMs. It may be desirable to use an on chip multiplier of a slow clock or an internal ring oscillator to transmit data at high frequency without a high speed clock for synchronization to reduce noise and system power. It will be appreciated
15 that those skilled in the art can build on the teachings of this invention to achieve various size, synchronous or asynchronous, high bandwidth systems.

The foregoing description of the preferred embodiments of the present invention is by way of example only, and other variations and modifications of the above-described embodiments and methods are possible in light of the foregoing teaching. For example,
20 although the system and method have been described as transmitting SSVTR and /SSVTR from a master 205 to a receiver 405, one skilled in the art will recognize that one reference may be sent and the complement generated on the receiver 405 side. Using the technique with other technologies, such as bipolar or gallium arsenide, which have

similar switching devices and gates, can alternatively be used. Components of this invention may be implemented using a programmed general purpose digital computer, using application specific integrated circuits, or using a network of interconnected conventional components and circuits. The embodiments described herein are not intended to be exhaustive or limiting. The present invention is limited only by the following claims.